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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/523,385	02/01/2005	Johannes Otto Voorman	NL 020728	4142

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EXAMINER	
LAMB, CHRISTOPHER RAY	
ART UNIT	**PAPER NUMBER**
2627	

DATE MAILED: 10/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/523,385	VOORMAN ET AL.	
	Examiner	Art Unit	
	Christopher R. Lamb	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 February 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The amendment to the drawings was received on August 11th, 2006. These drawings are not acceptable.

The new drawing is labeled "Fig. 3." However, there is already a Fig. 3 in the Application.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "low pass filter located between at least one sequential-logic circuit and said at least one analog adder/subtractor" (claim 5) must be shown or the features canceled from the claims. No new matter should be entered.

(Note the amended drawing received August 11th, 2006 was clearly intended to address this objection: however, because that drawing was improperly labeled, the amended drawing was not entered).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for

consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to because the unlabeled rectangular boxes shown in the drawings should be provided with descriptive text labels. Note that this objection has been repeated from the previous Office Action.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 1-5 are objected to because of the following informalities: in claim 1, line 6, the phrase "comprised of of at least" contains a redundant "of." Claims 2-5 are dependent on claim 1 and thus contain the same language. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 6, 7, 9, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishibashi et al. (US 5,808,979).

Regarding claim 1:

Ishibashi discloses an optical disk system (Fig. 1) comprising:

at least one photo detector comprising several sub-detectors for detecting at least a part of said optical disk (Fig. 1: 1; the sub-detectors are 1a-1d),

said at least one photo detector generating detection signals in response to said detection (Fig. 1: S_A to S_D),

the optical disk system further comprising several circuits (Fig. 1: one circuit comprises the chain of elements 2, 4a, 5a, 6a, 7a; the other 3, 4b, 5b, 6b, 7b),

each circuit having an input directly coupled to a respective output of one of said several sub-detectors for receiving said detection signals (Fig. 1: for the first circuit, element 2 is connected to at least one of the photodetectors; for the second, element 3 is),

said several circuits comprised of at least one amplifier for amplifying detection signals (Fig. 1: 5a and 5b contain amplifiers, as shown in Fig. 2A: they amplify detection signals S_2 and S_3) and

comprising at least one slicer for slicing amplified detection signals (Fig. 1: 7a and 7b),

the system further comprising at least one delay-difference detector for detecting delay differences in sliced amplified detection signals (Fig. 3: 1; Fig. 4),

characterized in that said delay-difference detector is delaylineless and comprises combinatorial-logic circuits and sequential-logic circuits (there are no delay lines in Fig. 4; 18 and 19 are combinatorial-logic circuits; 20 and 21 are sequential logic circuits).

Regarding claim 6:

All elements positively recited have already been identified with respect to claim 1.

Regarding claim 7:

The delay-difference detector of Ishibashi is characterized in that said delay-difference detector comprises a first pair of sequential-logic circuits for detecting delay differences between rising edges and a second pair of sequential-logic circuits for

detecting delay differences between falling edges (column 4, line 35 to column 5, line 10).

Regarding claim 9:

Ishibashi discloses a method for use in an optical disk system, comprising the steps of:

detecting at least a part of said optical disk using at least one photo detector comprised of at least several sub-detectors (Fig. 1: 1);

generating detection signals from said at least several sub-detectors, responsive to said detection (signals S_A and S_C are summed by element 2 and filtered by element 4a to become detection signal S_2; similarly for detection signal S_3);

independently amplifying said detection signals from each of said at least several sub-detectors to generate amplified detection signals (Fig. 1: 5a and 5b contain amplifiers, as shown in Fig. 2A; they act on signals S_2 and S_3);

slicing said amplified detection signals to generate sliced amplified detection signals (Fig. 1: 7a and 7b); and

detecting delay differences in said sliced amplified detection signals (Fig. 3: 1; Fig. 4);

wherein said detecting step of detecting delay differences is delaylineless (apparent from Fig. 4).

Regarding claim 10:

The method of Ishibashi is characterized in that said step of detecting delay differences comprises the sub-steps of detecting delay differences between rising edges and of detecting delay differences between falling edges (column 4, lines 35-63).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tateishi (US 6,775,210) in view of Ishibashi et al. (US 5,808,979).

Regarding claim 1:

Tateishi discloses an optical disk system (Fig. 1) comprising:

at least one photo detector comprising several sub-detectors for detecting at least a part of said optical disk (Fig. 1: 11),

said at least one photo detector generating detection signals in response to said detection (shown by the lines in Fig. 1),

the optical disk system further comprising several circuits, each circuit having an input directly coupled to a respective output of one of said several sub-detectors for receiving said detection signals (one circuit comprises element 12 of Fig. 1; the other circuit is element 13 of Fig. 1),

the system further comprising at least one delay-difference detector for detecting delay differences in detection signals (Fig. 1: 14; Fig. 2)

characterized in that said delay-difference detector is delaylineless and comprises combinatorial-logic circuits and sequential-logic circuits (there are no delay lines in Fig. 2; the invertors and/or gates are combinatorial-logic circuits; the flip-flops are sequential logic circuits).

Tateishi does not disclose:

that said several circuit are comprised of "at least one amplifier for amplifying detection signals and at least one slicer for slicing amplified detection signals."

Ishibashi discloses amplifiers for amplifying detection signals (Fig. 1: 5a, 5b) and slicers for slicing amplified detection signals (Fig. 1: 6a, 7b). Ishibashi discloses that these elements improve the signal-to-noise ratio of the signal (column 2, lines 10-25).

It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Tateishi at least one amplifier for amplifying detection signals and at least one slicer for slicing amplified detection signals, as taught by Ishibashi.

The motivation would have been to improve the signal-to-noise ratio.

Regarding claim 2:

Tateishi discloses that said delay-difference detector comprises a first pair of sequential-logic circuits for detecting delay differences between rising edges (Fig. 2: Q1 and Q2) and comprises a second pair of sequential-logic circuits for detecting delay differences between falling edges (Fig. 2: Q3 and Q4).

Regarding claim 3:

Tateishi discloses that said delay-difference detector further comprises at least one analog adder/subtracter for adding/subtracting sequential-logic circuit output signals (Fig. 1: 15, 16).

Regarding claim 4:

Tateishi in view of Ishibashi discloses an optical disk system as discussed above.

Tateishi in view of Ishibashi does not disclose "at least one low pass filter coupled to an output of said one analog adder/subtractor."

Ishibashi discloses at least one low pass filter coupled to an output of one analog adder/subtractor (Fig. 1: 9; the analog adder/subtractor is visible in Fig. 4). Ishibashi discloses that this filter smooths the difference signal (column 5, lines 11-14), helping achieve a high signal to noise ratio (column 2, lines 11-23).

It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Tateishi in view of Ishibashi at least one low pass filter coupled to an output of said one analog adder/subtractor.

The motivation would have been to achieve a high signal to noise ratio, as disclosed by Ishibashi.

Regarding claim 5:

Tateishi in view of Ishibashi discloses an optical disk system as discussed in claim 1 above.

Tateishi in view of Ishibashi does not disclose "at least one low pass filter located between at least one sequential-logic circuit and said at least one analog adder/subtracter."

Ishibashi discloses a low pass filter located after the phase comparator (Fig. 1: 9). Ishibashi discloses that this filter smooths the difference signal (column 5, lines 11-14), helping achieve a high signal to noise ratio (column 2, lines 11-23).

It would have been obvious to one of ordinary skill in the art to include in Tateishi in view of Ishibashi at least one low pass filter located after the phase comparator, and thus located between at least one sequential-logic circuit and at least one analog adder/subtractor (the sequential-logic circuits are instead Tateishi's phase comparator, and analog adder/subtractors 15,16 follow the phase comparator).

The motivation would have been to achieve a high signal to noise ratio, as disclosed by Ishibashi.

Regarding claims 6-8:

All elements positively recited have already been identified with respect to claim 1-3.

Regarding claims 9-10:

These are method claims corresponding to apparatus claims 1-5 and are met when the system operates. Note that since the amplifier was taught by Ishibashi, the same reasoning applied to the rejection of claim 9 under Ishibashi applies here in terms of "independently amplifying said detection signals."

Response to Arguments

9. Applicant's arguments filed August 11th, 2006 have been fully considered but they are not persuasive.

10. With regards to the drawing objection:

The Examiner acknowledges that the new drawing was intended to respond to the objection to the drawings for failing to show every feature of the invention specified in the claims. However, because the new drawing was labeled "Fig. 3" and there is already a "Fig. 3," the amended drawing was not entered.

The Examiner also points out that there was a second drawing objection in the previous Office Action which was not addressed by the Applicant. That objection has been repeated in this Office Action.

11. With regards to the rejection as anticipated by Ishibashi:

With regards to claim 1:

Applicant argument is essentially that the claim is allowable over Ishibashi because Ishibashi creates diagonal sum signals S_A+S_C and S_B+S_D and acts upon those signals rather than acting on the direct output of the photodetector.

However, as noted in the rejection above, Ishibashi still contains all elements of the claim. The claim does not forbid creating diagonal sum signals: it simply requires that "each circuit" have "an input directly coupled to a respective output of one of said several sub-detectors." The Examiner considers summing element 2 to be part of the first circuit, and summing element 3 to be part of the second circuit. It is clear in Fig. 1 that these elements are directly coupled to a respective output of one of the sub-detectors, and thus Ishibashi still meets the claim.

With regards to claim 6:

Applicant argues it is allowable because of its dependence on claim 1. Claim 6 does not appear to be dependent on claim 1. Regardless, it is similar to (although broader than) claim 1 and all elements of the claim have been identified in Ishibashi.

With regards to claim 9:

Applicant argues that it is allowable due to its similarity to claim 1. Note that the Examiner has used a slightly different interpretation of the detection signals of Ishibashi in order to reject this claim, as per the rejection above: nonetheless, Ishibashi contains all elements of the claim and thus this argument is not considered persuasive.

With regards to claim 10:

Applicant argues that is allowable due to its dependence on claim 9. As claim 9 has not been found allowable, this argument has not been found persuasive.

12. With regards to the rejection of claims 1-10 over Tateishi in view of Ishibashi:

Applicant only generally argued that the amendment has made the claims allowable over this combination. The Examiner has identified every element of the claims in the rejection over Tateishi in view of Ishibashi above; therefore, this argument was not found persuasive.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher R. Lamb whose telephone number is (572) 272-5264. The examiner can normally be reached on 8:30 AM to 6:00 PM Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Korzuch can be reached on (571) 272-7589. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CRL 10/17/06

William Korzuch

WILLIAM KORZUCH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

DO NOT ENTER
-CRL

Amendments to the Drawings:

See new drawing sheet, Fig. 3.

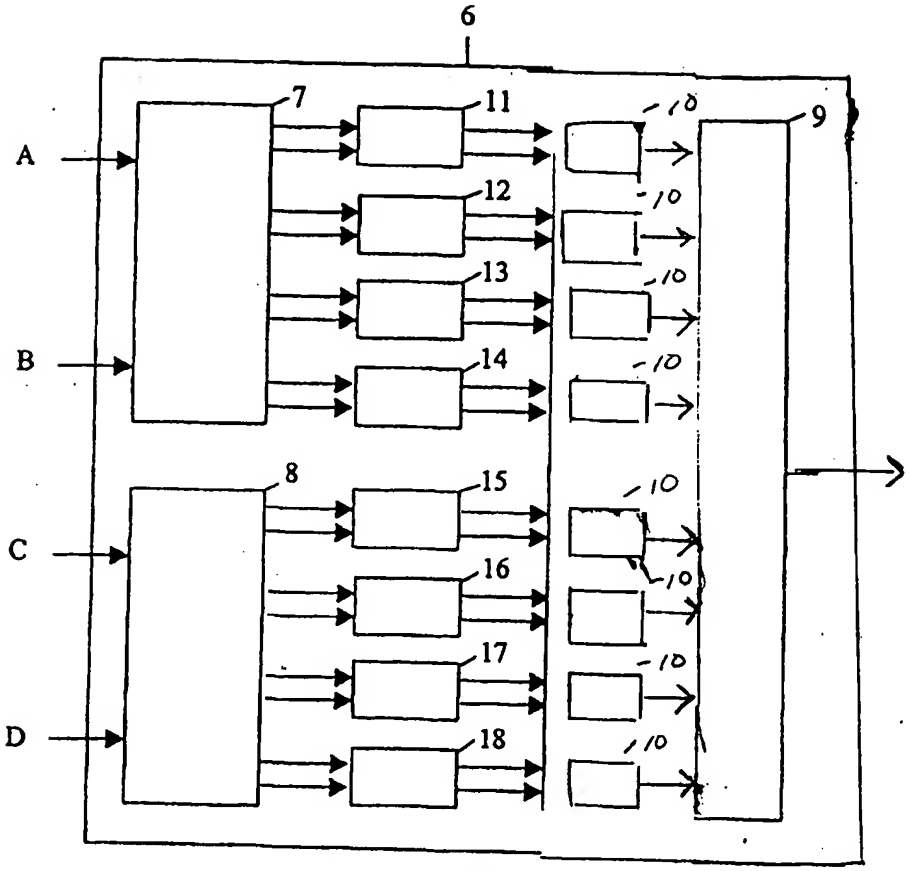

FIG. 3